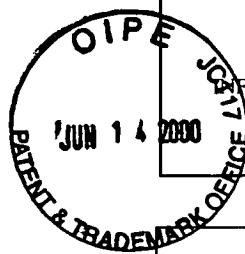


PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA001C10	SERIAL NUMBER 09/514,872
	APPLICANT(S) FARMWALD ET AL.	RECEIVED
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DA	4,330,852	May 18, 1982	Redwine et al.	—	—	
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DA	4,726,021	Feb. 16, 1988	Horiguchi et al.	—	—	
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
DA	S56-82961 ✓	July 7, 1981	Japan	—	—	YES
DA	S57-14922 ✓	Jan. 26, 1982	Japan	—	—	YES
DA	Sho 60-80193 ✓	May 8, 1983	Japan	—	—	YES
DA	Sho 60-55459 ✓	Mar. 30, 1985	Japan	—	—	YES
DA	S61-72350 ✓	April 14, 1986	Japan	—	—	YES
DA	S63-142445 ✗	June 14, 1988	Japan	—	—	YES
DA	B63-46864 ✓	Sept. 19, 1988	Japan	—	—	YES
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DA	0 334 552	Mar. 16, 1989	EPO	—	—	
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DA	4,747,079	03/24/88	Yamaguchi	—	—	
DA	4,649,511	03/10/87	Gdula	—	—	
DA	4,757,473	07/12/88	Kurihara et al.	—	—	
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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES NO

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DA	5,301,278	04/05/94	Bowater et al.	—	—	
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<i>DA</i>	4,821,226	04/11/89	Christopher et al.	—	—	
<i>DA</i>	4,882,712	11/21/89	Ohno et. al.	—	—	
<i>DA</i>	4,951,251	08/21/90	Yamaguchi et al.	—	—	
<i>DA</i>	4,928,265	02/29/92	Beighe et al.	—	—	
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<i>DA</i>	4,734,880	03/29/88	Collins	—	—	
<i>DA</i>	4,183,095	01/08/80	Ward	—	—	
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<i>DA</i>	T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul. Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
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PTO-1449 (Modified)		ATTY. DOCKET NO. RA001C10	SERIAL NUMBER 09/514,872	RECEIVED MAY 17 2000 2700
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PTO-1449 (Modified)		ATTY. DOCKET NO. RA001C10	SERIAL NUMBER 09/514,872
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JA	4,954,987	09/04/90	Auvinen et al.	—	—	
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JA	4,788,667	11/29/88	Nakano et al.	—	—	
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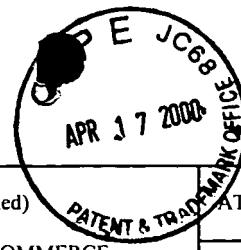
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JA	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
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